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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,196	08/26/2003	Huan-Ping Su	MM4635	6273

7590 11/23/2004

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,196	SU, HUAN-PING	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on 10/7/2004. These drawings are approved by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada (6,239,496) in view of, Tokuda et al. (5,870,289), Heo (6,555,917) and .Applicant Admitted Prior Art (AAPA).

Asada teaches in figure 3B and related text a flip chip semiconductor package, comprising:

a first chip carrier substrate or TAB 113 (column 6, line 51) mounted with at least a first chip 133 having a first active and non-active surfaces opposite each other wherein a plurality of first inner leads 723 are formed on the first active surface for electrically connecting the first chip to the first chip carrier;

a second chip carrier substrate 112 mounted with at least a second chip 132 having a second active and non active surfaces opposite each other wherein

a plurality of second inner leads 722 are formed on the second active surface for electrically connecting the second chip to the second chip carrier;

the first non active surface of the first chip is attached to second non active surface of the second chip;

a resin encapsulating layer 141-144, filled in between the first chip carrier and the second chip carrier for encapsulating the first chip, the second chip, and the first and second inner leads; and

a plurality of conductive vias 251-253 penetrating the first chip carrier and the second chip carrier so that the second chip carrier is electrically connected to the first chip carrier via the conductive vias.

Asada does not teach using solder bumps and an adhesive layer to attach the second chip to the first chip, wherein a plurality of conductive vias penetrating the resin encapsulating layer.

Asada teaches in the embodiment of figure 8B and related text using solder balls instead of inner leads.

Tokuda et al. teach in figure 4 a resin layer formed between first and second chip carriers and a plurality of conductive vias penetrating the resin encapsulating layer.

AAPA teaches on page 3 the advantages of using solder balls instead of inner leads.

Heo teaches in figure 8A and related text using an adhesive layer 28 to attach the second chip 10-3 to the first chip 10-2.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use solder bumps instead of inner leads and an adhesive layer to attach the second chip to the first chip wherein a plurality of conductive vias penetrating the resin encapsulating layer in Asada's device, in order to improve the reliability of the device and to provide better bonding between the two chips, respectively, and in order to use the device in an application which requires thicker chips. The combination is motivated by the teachings of AAPA which point out the advantages of using solder balls (page 3).
Note that using the device in an application which requires thicker chips would result in the first and second chip carriers being spaced apart from each other, and the resin encapsulating layer formed between the first and second chip carriers. Therefore, the conductive vias must penetrate the resin layer in other to communicate between the first and second chip carriers.

Regarding claim 2, Asada teaches in figure 8A a plurality of solder bumps are disposed on the exposed surface of the second chip carrier for forming electrical connection with another semiconductor package.

Regarding claims 5 and 10, Heo teaches in figure 8A an adhesive layer 28 being an insulating adhesive having high elasticity.

Regarding claim 6 and 11, Asada teaches in figure 3A and related text a resin encapsulating layer 141-144 being made of resin materials having low hygrosocopicity and low viscosity.

Regarding claim 7, Asada teaches in figure 3A and related text a plurality of conductive traces 121-124, 721-723 formed between the first chip carrier, the resin encapsulating layer, and the second chip carrier for electrically connecting the first chip to the first chip carrier via each of the conductive traces.

Regarding claim 8, Asada teaches in figure 3A and related text conductive traces have one end connected to the ball pads 153 of the second chip carrier and the other end connected to the ball pads 152 of the first chip carrier.

Regarding claims 13-16, the device of prior art includes conductive vias comprising a plurality of through holes opening through the first chip carrier, the resin encapsulating layer, and the second chip carrier, wherein a conductive layer is formed on an inner wall of each of the through holes to define a cavity, wherein the conductive layer is made of a copper foil, wherein the cavity is filled by a conductive material.

Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada, Tokuda et al., Heo and AAPA, as applied to claims 1, 7, 13 and 14 above, and further in view of Kim (5,407,864).

Asada, Tokuda et al., Heo and AAPA teach substantially the entire claimed structure, as recited in claims 1, 7, 13 and 14 above, except a cavity filled by a dielectric material, and a dielectric solder mask for encapsulating the conductive traces.

Kim teaches in figure 2F a cavity 9 filled by a dielectric material 14, and a dielectric solder mask for encapsulating the conductive traces 12.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to fill the cavity in prior art's device by a dielectric material, wherein a dielectric solder mask encapsulating the conductive traces, in order to provide high density method of mounting semiconductor chips with enhanced manufacturing characteristics.

Response to Arguments

Applicant argues that solder balls 641 or 654 of Asada are not equivalent to the claimed solder balls.

The examiner does not suggest that solder balls 641 or 654 of Asada are equivalent to the claimed solder balls. In fact, the examiner states that Asada does not teach using solder bumps to attach the second chip to the first chip. AAPA is cited to teach an artisan the advantages of using solder balls instead of inner leads.

The rest of applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308- 0956**

O.N.
11/17/04

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800